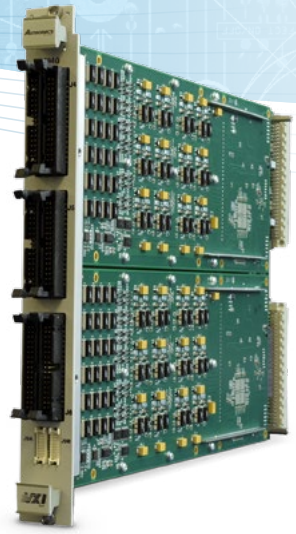
ASTRONICS TEST SYSTEMS



T940

50 MHz Digital Test Instrument

The Astronics T940 Series of Digital Test Instruments provides up to 64 high-performance digital I/O channels in a space-saving single-wide VXI 4.0 compatible module. The T940 Series operates at data rates up to 50 MHz with 1 ns edge placement, variable slew rates, and <3 ns channel-to-channel skew.

Product Information

The T940 Series for the VXIbus provides the basis for a complete state-of-the-art digital solution at the subsystem level. The T940 is *the* solution for both legacy digital replacement and new test stations to be built for digital test including aircraft/avionics, weapons systems, spacecraft, semiconductors and medical devices.

We reference the VXI 3.0 and 4.0 platforms to produce highly-capable and reliable digital subsystems that are backed by our proprietary digital sequencer architecture.

The T940 Series uses Field Programmable Gate Arrays (FPGA) and pin-driver technologies plus an advanced sequencer, to provide a choice of fixed or variable driver/receiver personality modules and create flexible digital instrumentation.

Mix and Match Driver/Receiver Modules for Value

When configuring a digital subsystem, combine an appropriate VXI mainframe/controller, configured T940 modules that include the Digital Test Instrument (DTI), your choice of Driver/Receiver (DR) daughter cards to meet the physical interface requirements, and software.

T940 Series features dual sequencers that can each operate in standalone or linked modes automatically with software commands.

DR card types include a full selection of variable-voltage and fixed-voltage types, including LVDS, LVTTL, and RS-485.

Applications for a Digital Subsystem

The T940 Series forms the backbone of a digital subsystem that may include switching, analog instrumentation, and even an RF subsystem.

The proven VXIbus instrumentation platform is a time-tested approach for facilitating the integration of these different technologies at the device level by allowing the free mixing of T940 modules with other VXI modules for added functionality. In addition, the T940 modules can be preintegrated at the subsystem level suited to a specific application.

KEY BENEFITS

- 50 MHz digital stimulus and response with 1 ns edge placement resolution
- Engineered for reliability with an advanced thermal design, temperature monitoring, and over-temperature shutdown
- Innovative software tools to speed test development
- Scalable design supports synchronized digital test systems from 24 to 768 channels
- High-speed data sequencer provides control of stimulus/response patterns
- Optional software tools simplify legacy replacement and preserve TPS investment

The Astronics Test Systems 1263 series and 1261B series mainframes, switching products, and other instrumentation integrate with the T940 Series to meet many stimulus/response needs.

Product Information (continued)

Astronics Test Systems offers custom design and integration services to create subsystems or fully integrated systems for functional testing on a variety of complex Devices Under Test (DUTs), including satellites, weapons systems, aircraft LRUs/SRUs, and certain classes of semiconductor devices.

From devices to turnkey systems, Astronics Test Systems can deliver all hardware and software solutions, including the Test Program Set (TPS) itself.

Designed for High Reliability

The T940 Series employs comprehensive thermal design to ensure reliability with excellent cooling, monitoring, and protection.

The pin electronics devices on the DR3/9 and UR14 employ a large heat sink, and there is also an on-board temperature monitor that protects the pin electronics from overheating and provides overtemperature shutdown.

An optional Astronics Test Systems 1263HP series high-power chassis provides the additional power and cooling required for large digital test systems.

Advanced Features for Modern Digital Test Development

The T940 Series' innovative design is suitable for today's challenging digital test system applications. The flexible FPGA design enables the T940 to meet special user and legacy requirements. The high-speed data sequencer provides control over test patterns, timing, and format.

Robust Protection Circuitry

All 24 V daughter-board channels can source and sink current as well as dissipate heat providing loading and high slew rates. To ensure that all channels are operating in a safe area, protection circuitry is provided for automatic fault condition detection. Figure 1 below summarizes the built-in protection features including overcurrent, overvoltage, and overtemperature monitoring (system cooling features are diagrammed). The digital bias power supply is also monitored for voltage faults.

Scalable Design

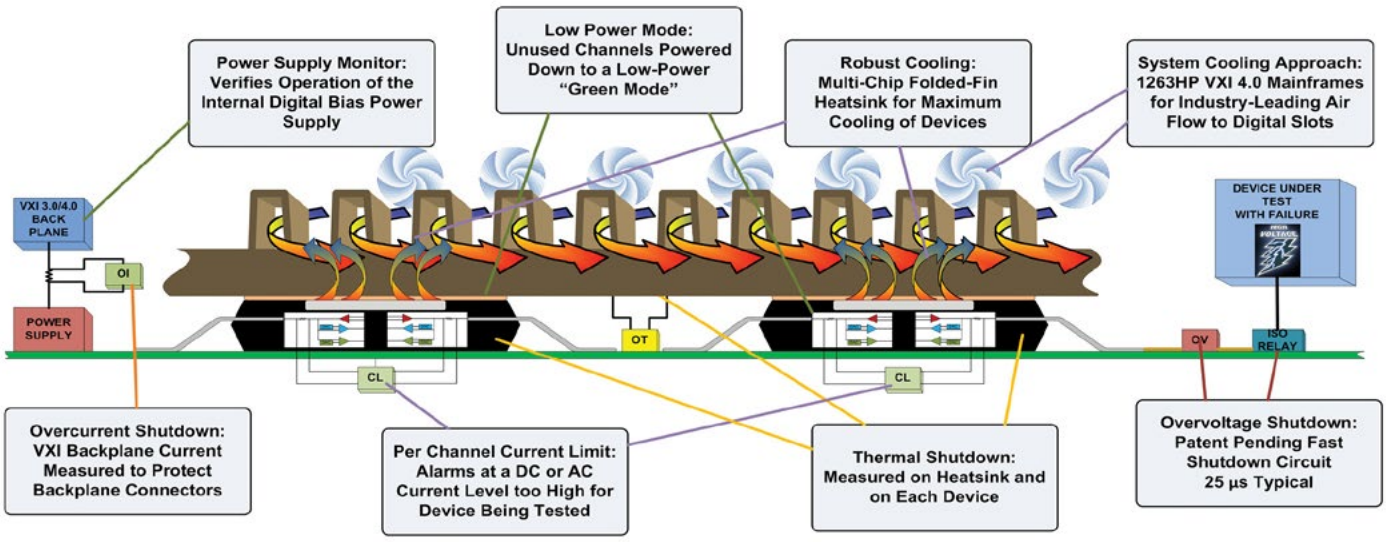
Built-in scalability and modular design enable configurations from 24 to 768 single-ended channels in 24 or 32 channel increments. Each T940 can hold up to two modules of 32 single-ended channels each.

Multiple T940 modules can operate both as independent 32-bit digital instruments or as a digital subsystem with up to 768 channels.

Triggering and Synchronization

The T940 Series features extensive control over digital testing to synchronize it with other test instruments and to control digital test sequencing.

The T940 accepts triggers from the VXI TTL Trigger Bus, VXI ECL Trigger Bus, Front Panel Auxiliary Inputs, or from any channel and provides two sync outputs per 32-channel module.



Product Information (continued)

Triggers can be used (1) to synchronize the T940 with other instruments; and (2) as a test input for test sequence control. Sync outputs can be offset to the start of a test sequence or step.

Efficient Use of Power

Two power conversion options are available to best take advantage of the available VXI backplane power sources. Power converters are provided when type DR3e, DR9, or UR14 driver/receiver modules are used.

The type 1 power (code -001) converter is available for use with a traditional VXI 3.0 mainframe. For this type, backplane current is limited to what can be provided by the standard VXI 3-row connector, and channels will shutdown if maximum power is exceeded.

The type 3 power converter (code: -003) is also available for systems using the 1263HPx VXI 4.0 mainframes. Type 3 takes advantage of VXI 4.0 power distribution, allowing the module to provide additional power, compared to type 1, without reaching its limit.

High-Speed Data Sequencer

The high-speed data sequencer provides control over digital test patterns. Each DTI contains two data sequencers that can operate independently or synchronously for timing, memory, and control of the two front-end modules.

Sequencer logic supports full UUT handshaking and controls timing, format, pattern data, looping, and conditional testing. The sequencer includes definable standby and idle sequences.

Variable Voltage DR Modules

The DR3e and DR9 modules provide 32 and 24 single-ended channels in a single plug-in module. Each T940 DTI can accommodate up to two modules for up to 64 or 48 single-ended channels in a single VXI slot. The DR9 modules include an analog port for each channel for connection to an instrument matrix, for example.

Variable voltage modules such as the DR3e and DR9 feature:

- Six voltage ranges from -15 V to +24 V with an output swing of up to 24 V
- Full drive current on all channels simultaneously when used with our 1263HP series mainframes
- Programmable current load with dual commutating voltages
- Programmable resistive input load to a programmed voltage
- Program slew rates selectable per channel (0.2 V/ns to 1.3 V/ns, typical)
- 12/50 Ω selectable output impedance
- Real-time over-voltage protection on each channel
- Robust protection circuitry for the entire module as shown in the previous diagram

Fixed Voltage DR Modules

There are currently three different fixed voltage DR modules available for the T940 Series:

- DR1: Low-Voltage TTL Digital I/O
- DR2: Low-Voltage Differential Signaling (LVDS) Digital I/O
- DR7: RS-485 Differential Digital I/O

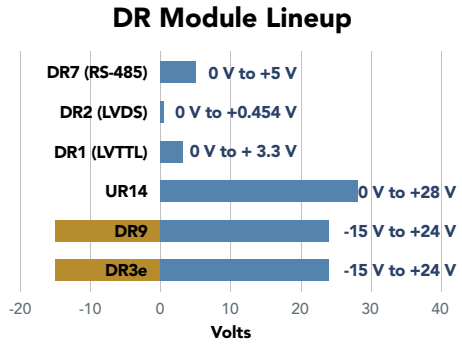


Figure 2: Available DR Modules

T940 Soft Front Panel (SFP)

The SFP provides interactive control of the T940 digital subsystem. The easy-to-use graphical interface enables setup and configuration, calibration, and sequencer control. Channels may be set up either individually or in user-defined groups.

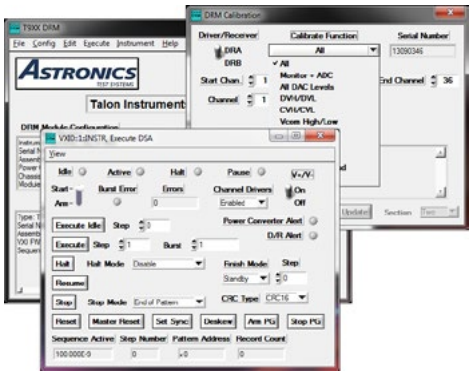


Figure 3: Soft front panel

Using the SFP, users are able to define and debug digital tests. The SFP also has the ability save digital tests for later use by the SFP or programmatically within test sets.

Product Information (continued)

Digital Functional Language (DFL)

The optional DFL provides a high level programming interface to the T940, providing the capability for you to seamlessly utilize the T940 Series with legacy test programs. This interface enables the T940 to emulate the legacy system characteristics without changing the underlying C program that executes the digital test.

Application Resource Interface (ARI)

The optional ARI also provides an interface to legacy systems from the T940 for you to seamlessly utilize the T940 with legacy test programs. The ARI provides a higher level of control of the advanced features within the T940 compared with those in DFL which is primarily used to emulate the legacy digital subsystem.

Innovative Software Tools Speed Test Development

The VXI*plug&play* driver and digital resource suite application interface layer support third-party test development tools to ease development and integration into popular test environments.

The optional Microsoft® Windows® CIIL Emulation Module (WCEM) for TYX PAWS® Run Time System (RTS), one of the most popular independent implementations of the ATLAS language, provides an interface to the T940 from the IEEE standard ATLAS test language for modern test development. This interface provides support for both legacy and modern system implementations that take advantage of the higher order, signal-oriented features of IEEE ATLAS.

The optional TestCue runtime package also provides a digital test development and debug environment that is designed to be used with National Instruments TestStand.

The Digital Programming support enables developers to access the T940 digital features directly within TestStand without having to use other IDE environments for programming.

Subsystem Configurations

Subsystems are configured contiguously across the VXI 3.0 or 4.0 backplane slots in a right-to-left sequence with the master module located in the right-most slot and with slave modules linking together with the master in a leftward direction.

Legacy Replacement Configurations

The T940-UR14 replaces a legacy central resources board.

The T940-DR9-DR9 replaces legacy variable-voltage I/O cards with 48 analog test channels.

The T940-DR3e-DR3e replaces 64-channel legacy variable-voltage cards when analog test channels

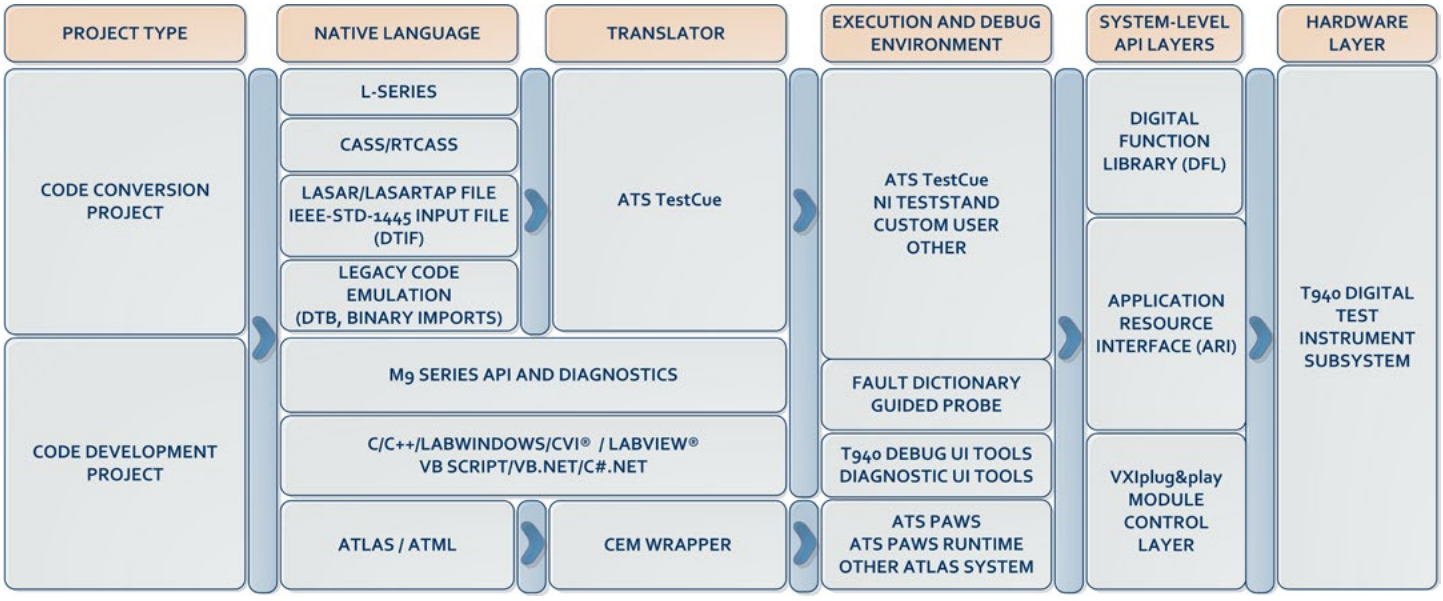


Figure 6: Third-party test development tools

Product Information (continued)

are not required. The T940-DR3e-DR3e can be used with or without the T940-UR14 as master because it can provide its own probe, clock, and external pause/halt I/O.

Specifications

Note: The Astronics Test Systems policy is one of continuous development and improvement. Consequently, the equipment may vary in detail from the description and specifications in this publication.

Please contact Astronics Test Systems for more information on how to configure a synchronized digital test system and for the expected performance characteristics of specific system configurations.

Timing Characteristics

I/O Data Rate

- Up to 50 MHz

Timing Set Options (3)

- 256 Timing Sets with 4 Phases and 4 Windows and 4 k sequence steps
- 1 k Timing Sets with 4 Phases and 4 Windows and 1 k sequence steps (one for each Seq. Step)
- 4 k Timing Sets with 1 Phase and 1 Window and 4 k sequence steps (one for each Seq. Step)

Phase/Window/Period Timing Resolution

- 1 ns (using the 500 MHz master clock)

Minimum Phase/Window Pulse Width

- 8 ns (using the 500 MHz master clock)

Clocks per Pattern (CPP)

- 1 to 256 (selectable per Seq. Step)

Pause-Resume Feature

- Phases and Windows are frozen when asserted.

Halt-Resume Feature

- All Phases will complete their action for the current Pattern.

Stimulus/Capture Characteristics

Testing Modes

- Dynamic, Static

Data Output Formats (per channel)

- Force: lo, hi, tri-state
- Format: NR, RT, R0, R1, RC, Complement Surround. Output the Phase or its complement (used to output Waveforms on channels)

Capture Modes (per channel)

- Mask
- Opening edge of window
- Closing edge of window
- Window (input data must match "expect" for the entire duration of the window).

Pattern Memory

- Size: 256 k

Pattern (Stimulus/Expect) Data

- Output: H, L, Tristate
- Expect: Good 1, Good 0, OK , between or mask
- Keep last
- Toggle last
- Accumulate a CRC16 or CRC32 (based on a Good 1 only)

Recording Mode

Recording Modes (per sequence step)

- Record errors for programmable inputs that have a Good 1 and Good 0
- Record errors for single-ended inputs that have only a Good 1
- Record raw data based on NOT a Good 0
- Record raw data based on a Good 1

Sequencer Characteristics

General

- Sequencers: 2 per Digital Resource Module
- Channels: 32 per sequencer
- Modes: Static, Dynamic

Sequence Memory

- Sequence Size: 1024 or 4096 Steps

Sequence Loop Counters

- Loop Counters: 16
- Loop Count can be different each time or continuous.
- Loop counters may be nested.
- Loop counters can be optionally re-loaded during a burst.
- Only one can end on a sequence step.

Specifications (continued)

Loop Count Range
- 1 to 64 k or continuous

Subroutine Characteristics
- Output one or more Sequence Steps with or without looping. Cannot be nested. Has a designated "Return" Step.

Burst Count Range
- 1 to 1 M or continuous

Jump Types
- Conditional or unconditional
- Jumps at the end of a sequence step
- Vectored (1 of 16 destinations)

Sync Pulse Outputs
- Outputs per Sequencer: 2
- Modes: Start of Sequence, Start of Sequence Step
- Offset Range: 0 to 1 M patterns
- Pulse Width: 1 to 4095 patterns

Sequence Standby Characteristics
- A one word continuous Sequence Step that may be used to output "standby" data on power up or after a sequence reset. The CPU can access pattern data in this state.

Idle Sequence Characteristics
- A continuous Sequence Step that may be used to output data before or after an active sequence. The CPU cannot access pattern data in this state. The Idle Sequence output after the active sequence may be different from the one output before.

Timer/Counter Characteristics
- Frequency Range: 0.25 Hz to 250 MHz
- Aperture Window Accuracy: ±50 ppm
- Preset Aperture Windows: 1 ms to 10 s in decade steps

Master Clock

Internal Oscillator
- 500 MHz
- Accuracy: 50 ppm

Internal Synthesizer
- 40 kHz to 500 MHz
- Accuracy: 50 ppm

Internal Reference
- 20 MHz or VXI CLK10

External Front Panel Reference
- Range: 5 to 80 MHz

DR1

Digital I/O Type
- DR1: LVTTL

Channels
- 32 SE per I/O board
- 64 per VXI slot
- Per channel relay isolation

Output Voltage (DR1)
- VOL: 0.55 V (max)
- VOH: 2.4 V (min)

Output Drive Current
- DR1: Source/Sink: 24 mA (typical)

Output Impedance (Program selectable per pin)
- Direct or 100 Ω (-x01)
- Direct or 50 Ω (-x02)

Input Impedance (DR1) (Program selectable per pin)
- 100 Ω pull-up to Vcc
- 100 Ω pull-down to ground
- (Ch 1 to 32, Aux1 to 4 only)

Skew (Channel-to-channel)
- <3 ns (drive and compare)

Auxiliary I/O Channels (per I/O board)
- DR1: LVTTL (8)
- ECL (4): Single Ended or Differential
- Per channel relay isolation

Data Rate (max)
- 50 MHz (input and output)

DR2/DR7 Characteristics

Digital I/O Type
- DR2: LVDS
- DR7: RS-485

Channels
- 32 Differential per I/O board
- 64 per VXI slot

Differential Output Voltage
- DR2: 454 mV (max); 247 mV (min)
- DR7: 3.0 V (max); 2.0 V (min)

Output Drive Current (typical)
- DR2: Source/sink ±8 mA
- DR7: Source/sink ±60 mA

Specifications (continued)

Output Impedance
- 100 Ω in parallel
  (contact factory for other options)

Skew (Channel-to-channel)
- <3 ns (drive and compare)

Auxiliary I/O Channels (per I/O board)
- DR2: LVDS (4), Differential
- DR7: RS-422/485 (4)
- LVTTL (4), Single-Ended
- ECL (4): Single Ended or Differential
- Aux I/O is bi-directional
- Per channel relay isolation on ECL I/O

Data Rate (max)
- DR2: 50 MHz (input and output)
- DR7: 10 MHz (input and output)

DR3e/DR9 Characteristics

Digital I/O Type
- Variable Voltage

Channels
- DR3e: 32 SE or 16 DIFF per I/O board
- DR9: 24 SE or 12 DIFF per I/O board and 24 analog test channels
- Per channel relay isolation

Analog Test Channels (DR9)
- Voltage Rating: 200 V max
- Current Rating: 1 A (carry), 0.5 A (switching)
- Frequency Range: 0 to 100 MHz

Channel Connectors
- DR3e: MDR-100 x 2
- DR9: IDC, 34-pin, 1 per 16 channel pins or analog test pins

Output Drive Current
- ±85 mA typ (Source/Sink)

Output Impedance (Program selectable per pin)
- 12 Ω or 50 Ω ±4 Ω

Slew Rate (Programmable per Pin)
- 0.2 V/ns, 0.7 V/ns, 1.0 V/ns, or 1.3 V/ns (typ)

Input/Output Threshold/Voltage Ranges
- 0 V to +24 V
- -5 V to +7 V
- -5 V to +15 V
- -10 V to +10 V
- -12 V to +12 V
- -15 V to +5 V
  (24 V max swing)

Skew (Channel-to-channel)
- <3 ns (drive and compare)

Current Source/Sink (DR3/DR9)
- ±0.4 mA to ±24 mA

Commutating Voltage: Vcom (Dual)
- DR3/DR9 Range: same as driver

Resistive Loads (DR3/DR9)
- 140 Ω to ~1 kΩ (8 selections) to Vcom

Ground Reference Input (per I/O board)
- Offset: ±3 V
- Interrupt Voltage: 390 mV
- Resistive load: 100 kΩ
- Bypass Relay: On or Off

Pin Electronics Monitoring (per channel)
- All programmed levels
- Output and Input levels
- Temperature

Auxiliary I/O Channels (per I/O board)
- DR3e only:
  - Programmable Level (4)
  - LVTTL (4)
  - ECL (4) single-ended or differential
  - Per channel relay isolation

Data Rate (max)
- 50 MHz (input and output)

UR14 Characteristics

Digital I/O Type
- High-voltage utility pins
- Over-voltage and over-current protection

Channels
- 32 bi-directional channels per VXI slot

Output Voltage (typical)
- Open Collector Output Voltage Range: 30 V
- Threshold Range: 0 V to 20 V
- Input Threshold Resolution: 5 mV

Output Current
- Up to 1 A per group of 8 channels
- Overcurrent Protection: Programmable

Specifications (continued)

Measurement Capability (per channel)

- System Meter
  - Range: -10 V to +15 V

Auxiliary Functions

- Programmable Level (6) (2 are dedicated to the Probe, when used)
- LVTTL or SE/DIFF ECL (4)
- LVTTL of SE ECL (4)
- SE/DIFF ECL (3)
- LVTTL (2)
- Probe Interface port

Channel Data Rate (max)

- Output: <5 kHz
- Input: <500 kHz

External Probe Module

Probe Tip Characteristics

- Input capacitance: <20 pF
- Input impedance: 10 MΩ ±1%

Contact Detect

- <5 MΩ or >50 pF
- Illuminates the green LED on the Probe Handle when contact is made
- Contact LED will extinguish while a pattern burst is in progress

Analog Performance

- Input voltage detectable range: -19 V to +19 V
- Input voltage absolute maximum rating: -200 V to +200 V

Timing Performance

- Absolute accuracy: ±5 ns with respect to Channel 1

Minimum pulse width:

- 10 ns

Buffered probe output

- Provided on the UR 14 as PROBE OUT
- Output range: Same as input from the Probe Module
- Output Impedance: Source terminated at 50 Ω in the Probe Module
- Output accuracy from the Probe tip to terminated output: ±(50 mV + 1%)

Interface

Front Panel I/O

Digital I/O

- DR1, DR2, DR3e, and DR7 I/O Boards:100 pin 3M MDR Connector (1 per I/O board)
- DR9: 34-pin IDC connector (1 per each set of 16 digital or analog test channels)
- UR14: 50-pin (2), 20-pin (2) and 26-pin (2) IDC connectors

Mating Connector Options

- DR1, DR2, DR3e, and DR7 I/O Boards:100 pin 3M MDR Mini Ribbon Connector or Backshell mounted Coaxial I/O launchers (1 per I/O board)
- DR9: 34-pin IDC ribbon or coaxial launchers
- UR14: 50, 20, 26-pin IDC ribbon. Coaxial for probe cable (26-pin IDC)

VXI Interface

Bus Operation

- VXI Register-based, D32/A32, VXI 4.0 transfer modes are available
- Message-based interface is available.

Backplane Operation

- CLK10 and CLK100: Clock reference
- LBUS: Multi-module synchronization
- TTL Trigger Lines: Sequence triggers

Software

Native Language

- C, ATLAS, ATML

Driver Support

- 2 Level: 1 @ card VXIpnp type driver; 1 @ system API type driver

Environmental

Temperature

- Operating: 0° C to 45° C
- Storage: -40° C to 70° C

Humidity (non-condensing)

- 0° C to +10° C: Not controlled
- +10° C to +30° C: 5 to 95 ±5% RH
- +30° C to +40° C: 5 to 75 ±5% RH
- +40° C to +50° C: 5 to 55 ±5% RH

Specifications (continued)

Emissions/Immunity

- EN61326:2006 Class B (pending)

Safety

- EN61010-1:2010-06 (pending)

Mechanical

Dimensions

- Single slot, C-size VXI module 10.2" H x 13.8" W x 1.2" D (260 mm x 350 mm x 30 mm)

VXI 4.0 Connectors

- 5-row VXI 4.0 P1 and P2, backwards compatible with VXI 3.0 3-row connector

Ordering Information

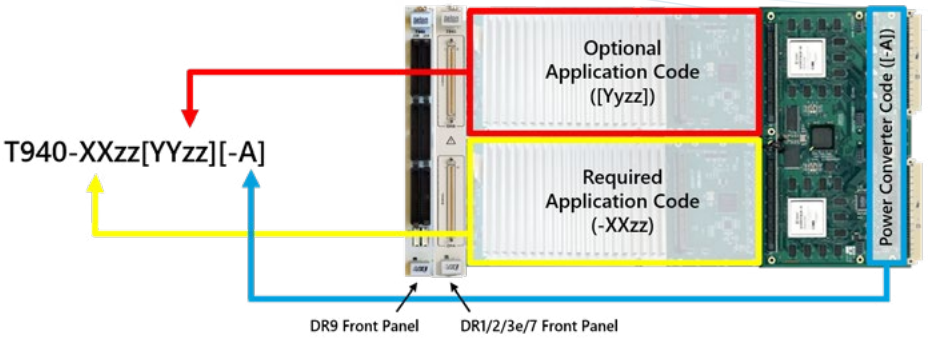
T940-XXzz[-YYzz][-A] : Astronics Test Systems T940 Digital Test Instrument

Digital Test Instrument Configured System

To create the 2nd, 3rd, and 4th sections of the part # for a configured T940, substitute the "-XXzz," "-YYzz," and [-A] in the part # with

the correct Application and Power Converter Code from the table below. Note that the rightmost front panel is representative of the

DR1/2/3e/7 modules. The leftmost front panel shown is for the DR9 and is similar in style to the T940-UR14 front panel.



MODEL	CODE (-XXZZ) (-[YYZZ])	APPLICATION CODE DESCRIPTION SPARES PART #	SPARES PART #
DR1	0150	LVTTL, 32 Channels, 50 Ω source termination	405349-002
DR1	0110	LVTTL, 32 Channels, 100 Ω source termination	405349-001
DR2	0210	LVDS, 32 Channels, 100 Ω source termination	405350
DR3e	3e50	Variable Voltage, -15 V to +24 V, 32 Channels, Over-voltage	408002
DR7	0710	RS-422, 32 Channels, 100 Ω source termination	405350-101
DR9	0950	Variable Voltage, -15 V to +24 V, 24 Direct/Analog Test Channels	408248
UR14	1450	Utility Resource, 32 HV Open Collector channels, probe interface, auxiliary interface	408291

MODEL	CODE (-XXZZ) (-[YYZZ])	APPLICATION CODE DESCRIPTION SPARES PART #	SPARES PART #
N/A	1	VXI 3.0 power converter	405404-001
N/A	3	VXI 4.0 power converter	405404-003

Part Number Ordering Examples:

T940-3e503e50-3	T940 with two sets of 32 DR3e variable-voltage channels and a VXI 4.0 augmented power converter
T940-3e50-1	T940 with 32 DR3e variable-voltage channels and a VXI 3.0 power converter

Additional Ordering Information

408177-001 : Racal Instruments™ 1263HPf High Power VXI 4.0 mainframe, front-maintainable

408177-005 : Racal Instruments™ 1263HPr High Power VXI 4.0 mainframe, rear-maintainable

Accessories:

602715-XXX : T940 coaxial IDC cable, 17 positions, both ends IDC-terminated (4 per 64 channel module, used with the DR9 module)

408122-XXX : T964/302-XXX Front Panel Signal Flat Shielded Cable (1 per Driver/Receiver Board) Dual-terminated

408123-XXX : T964/300-XXX Front Panel Signal Flat Ribbon Cable (1 per Driver/Receiver Board) Dual-terminated

Key: XXX = length in feet

405389-001 : Diagnostic Probe Board, Panel Mount

405389-002 : Diagnostic Probe Board, Flush Mount

408378-XXX : UR14 or UR14 Funnel (408257) Diagnostic Probe Cable

Key: XXX = length in inches

408257 : Funnel, VP90 Coaxial Interface, T940-UR14

408258 : Funnel, VP90 Coaxial Interface, T940-DR9

Software Licenses:

N/A : Driver/Soft Front Panel (included with base Digital Test Instrument)

T940-WCEM : Windows® CIIL Emulation Module for TYX PAWS™ ATLAS Runtime System (one license per T940 system)

T940-ARI : Application Resource Interface (ARI, one license per T940 system)

T940-TC-DIAG: T940 Diagnostic Suite (Guided Probe and Fault Dictionary, one license per T940 system)

T940-TC-GP: T940 Guided Probe (one license per T940 system)

T940-Fault-Dict-SW: T940 Fault Dictionary (one license per T940 system)

T940-TC-LSR: LASAR to T940 High Speed Digital Post Processor (one license per T940 system)

T940-TC-M9: TerM9 Library including Binary Reader

T940-TC-DTB: Binary Reader for DTB and Diagnostic files

T940-TC-LSR-GP: LASAR to T940 Guided Probe (one license per T940 system)

CONTACT

4 Goodyear
Irvine, CA 92677 USA
+1.949.859.8999 | 800.722.2528
ATSsales@astronics.com
astronicstestsystems.com